UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/785,073	02/25/2004	Teruo Takizawa	118439	8936

25944 7590 08/11/2006

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
QUINTO, KEVIN V	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 08/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/785,073	TAKIZAWA, TERUO	
	Examiner	Art Unit	
	Kevin Quinto	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-6 and 8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-6 and 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1, 2, 4, 5, 6, and 8 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 4, and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi (United States Patent Application No. US 2003/0197598 A1) in view of Udrea (USPN 6,111,289) and further in view of Huang (United States Patent Application Publication No. US 2003/0102534 A1) and further in view of DiBuganara (USPN 4,126,713).

4. With regard to claims 1 and 4, Hayashi (United States Patent Application No. US 2003/0197598 A1) discloses a similar device. Figures 9 and 10 of Hayashi disclose a semiconductor device with a bridge rectifier circuit (3 in figure 9, figure 10 has added detail) having a plurality of diodes (D1-D4, figure 10) which rectify a predetermined alternating-current voltage to a direct-current voltage. Hayashi does not disclose the use of a diode formed on an insulating substrate having using a p-type silicon layer and

an n-type silicon layer. However the use of such diodes is well known in the art. Udrea (USPN 6,111,289) discloses a diode with p-type silicon layer joined to an n-type silicon layer both of which are disposed on an insulating substrate in figure 1. In figure 1 of Udrea, there is a p-type silicon layer joined to an n-type silicon layer which are both disposed on the insulating substrate. Udrea states that the diode of figure 1 has the benefit of a larger breakdown voltage compared to conventional diodes (column 2, lines 45-49). Udrea makes it clear that semiconductor devices with large breakdown voltages are a known goal in the semiconductor art (column 1, lines 7-14). In view of Udrea, it would therefore be obvious to implement the Udrea diode in the bridge rectifier circuit of Hayashi. Udrea does not disclose using p-type silicon with germanium for the anode of the diode. However the use of such materials in a diode is well known in the art. Huang (United States Patent Application Publication No. US 2003/0102534 A1) discloses that the use of p-type silicon with germanium for the anode in a diode gives it the benefit of a reduced reverse recovery time (p. 1, paragraphs 10-11). DiBuganara (USPN 4,126,713) discloses that the reduction of reverse recovery time in diodes is a known goal in the art (column 1, lines 16-25). In view of Huang and DiBuganara, it would therefore be obvious to use p-type silicon with germanium as the anode in the diode of Udrea.

5. With regard to claim 5, figure 9 of Hayashi shows that the semiconductor device has a coil antenna (L1) coupled to one side of the bridge rectifier circuit (3); a smoothing capacitor (Ca) coupled to the other side of the bridge rectifier circuit (3). The coil antenna (L1) generates an alternating-current voltage by electromagnetic induction.

The bridge rectifier circuit (3) rectifies the alternating-current voltage into a direct-current voltage. The smoothing capacitor (Ca) smoothes the direct-current voltage into a constant voltage.

6. Claims 2 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hayashi (United States Patent Application No. US 2003/0197598 A1) in view of Omura et al. (USPN 6,049,109) and further in view of DiPiazza (United States Patent Application Publication No. US 2003/0137284 A1) and further in view of Streetman ("Solid State Electronic Devices," p. 205) and further in view of Huang (United States Patent Application Publication No. US 2003/0102534 A1) and further in view of DiBuganara (USPN 4,126,713).

7. With regard to claims 2 and 8, Hayashi (United States Patent Application No. US 2003/0197598 A1) discloses a similar device. Figures 9 and 10 of Hayashi disclose a semiconductor device with a bridge rectifier circuit (3 in figure 9, figure 10 has added detail) having a plurality of diodes (D1-D4, figure 10) which rectify a predetermined alternating-current voltage to a direct-current voltage. Hayashi does not disclose the use of PIN type diodes in the circuit which uses a p-type silicon layer, an intrinsic silicon layer, and an n-type silicon layer. However the use of such diodes is well known in the art. Omura et al. (USPN 6,049,109, hereinafter referred to as the "Omura" reference) discloses a PIN diode on an insulating substrate in figure 1. In figure 1 of Omura, there is a p-type silicon layer (95) which is joined to an intrinsic silicon layer (93). An n-type silicon layer (94) is joined to the intrinsic silicon layer (93). The p-type silicon layer (95), intrinsic silicon layer (93), and the n-type silicon layer (94) are all disposed on the

insulating substrate (92). DiPiazza (United States Patent Application Publication No. US 2003/0137284 A1) states that PIN diodes are known to have a fast switching time (p.1, paragraph 4). Streetman ("Solid State Electronic Devices," p. 205) states that diodes with a fast switching speed are desirable in the art. In view of DiPiazza and Streetman, it would therefore be obvious to implement the Omura diode in the bridge rectifier circuit of Hayashi. Omura does not disclose using p-type silicon with germanium for the anode of the diode. However the use of such materials in a diode is well known in the art. Huang (United States Patent Application Publication No. US 2003/0102534 A1) discloses that the use of p-type silicon with germanium for the anode in a diode gives it the benefit of a reduced reverse recovery time (p. 1, paragraphs 10-11). DiBuganara (USPN 4,126,713) discloses that the reduction of reverse recovery time in diodes is a known goal in the art (column 1, lines 16-25). In view of Huang and DiBuganara, it would therefore be obvious to use p-type silicon with germanium as the anode in the diode of Omura.

8. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Udrea (USPN 6,111,289) and further in view of Huang (United States Patent Application Publication No. US 2003/0102534 A1) and further in view of DiBuganara (USPN 4,126,713) and further in view of Beasom (United States Patent Application Publication No. US 2003/0071291 A1) and further in view of Shopbell (USPN 6,055,460) and further in view of Farber et al. (USPN 6,187,684 B1).

9. In reference to claim 6, Udrea (USPN 6,111,289) discloses a similar method of manufacturing a semiconductor device. Udrea discloses a diode with p-type silicon

layer joined to an n-type silicon layer both of which are disposed on an insulating substrate in figure 1. Udrea does not disclose using p-type silicon with germanium for the anode of the diode. However the use of such materials in a diode is well known in the art. Huang (United States Patent Application Publication No. US 2003/0102534 A1) discloses that the use of p-type silicon with germanium for the anode in a diode gives it the benefit of a reduced reverse recovery time (p. 1, paragraphs 10-11). DiBuganara (USPN 4,126,713) discloses that the reduction of reverse recovery time in diodes is a known goal in the art (column 1, lines 16-25). In view of Huang and DiBuganara, it would therefore be obvious to use p-type silicon with germanium as the anode in the diode of Udrea. Udrea does not disclose forming the silicon-germanium mixed crystal by implanting germanium to the p-type silicon layer. However this method of forming silicon germanium is well known in the art. Beasom (United States Patent Application Publication No. US 2003/0071291 A1) discloses that using ion implantation (implanting germanium into silicon) in order to form silicon germanium is a known method (p.4, paragraph 39). Furthermore Shopbell (USPN 6,055,460) discloses that ion implantation has the benefit of taking place in a clean environment (column 6, lines 35-38). Farber et al. (USPN 6,187,684 B1, hereinafter referred to as the "Farber" reference) discloses that fabrication in a clean environment is desired in the semiconductor art (column 2, lines 23-26). In view of Beasom, Shopbell, and Farber, it would therefore be obvious to utilize ion implantation as the means of forming the silicon germanium mixed crystal.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KVQ